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A Fast Settling Multi-Standard CMOS Fractional-N Frequency Synthesizer for DECT/GSM/ CDMA &/NADC Wireless Communication Standards

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ABSTRACT

A fast settling multi-standard CMOS fractional-N frequency synthesizer for DECT, GSM, CDMA and NADC wireless communication standards is proposed. This frequency synthesizer was simulated with ADS2008 in TSMC RF CMOS 0.18 µm. Frequency range is 824-1900 MHz, a switched capacitor LC-VCO was used in order to produce this frequency range. Frequency synthesizers have three main specifications of phase noise, settling time and power consumption. A new channel select circuit was designed instead of ∑Δ modulator to locate spur tones far from center frequency. A high reference frequency was used in order to reduce the VCO phase noise and locate the spur tones far from center frequency; these tones are produced by charge pump (reference spur) and N/N+1 divider (fractional spur). Two ways were used for phase noise optimization; in the first way phase noise was reduced by a low pass filter and a bypass capacitor (CT) that eliminate thermal noise and $2\omega_0$ harmonics of tail current source; in the second way with biasing of VCO transistors only in saturation region preventing reduction of quality factor(Q) in tank circuit. These two ways in VCO of DECT were used, consequently the phase noise at 1875MHz center frequency was improved from -119.4 dBc/Hz at 3.4 MHz offset frequency to -144.3 dBc/Hz at 3.4 MHz offset frequency. The settling time for all standards was achieved less than almost 1 µs over the entire frequency range. For DECT synthesizer phase noise of -116.37 dBc/Hz at 3 MHz offset frequency was obtained, the first spur tone was located in 7.35 MHz offset from center frequency, also settling time of 350ns was obtained. The whole frequency synthesizer in loop1 (for DECT) draws 13 mA and in loop2 (for GSM900, CDMA & NADC) draws 13.67 mA from a 1.8 V voltage supply.

Keywords: Phase Lock Loop (PLL), Phase noise, Charge pump, Voltage Controlled Oscillator (VCO), Channel select circuit, Programmable divider

Introduction

Nowadays wireless media is used more and more for voice and data communications; consequently higher integration in transceivers is needed in order to achieve lower cost, smaller size and lower power dissipation. In higher integration level in addition to high substrate noise, on chip components should be used that have lower Q than off chip component, therefore the structure of transceivers should be optimized in order to reduce noise [1].

Numerous standards exist which are optimized for different applications; for example DECT, GSM, CDMA and NADC are used for voice, but 802.11 WLAN or Bluetooth are used for data communications. Synthesizers are used in transceivers to produce standard frequencies for mixers. There are different type of frequency synthesizers; Direct Digital Synthesizer (DDS), Direct Analog Synthesizer (DAS) and PLL based synthesizer such as integer-N frequency

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synthesizer, fractional-N frequency synthesizer and dual loop frequency synthesizer. A standard tells how devices talk to each other. There are three main specifications of phase noise, settling time and power consumption in frequency synthesizers. In this paper, design and simulation of a fractional-N frequency synthesizer for DECT, GSM900, CDMA and NADC wireless standards is proposed so that provides standard requirements. Two Phase Lock Loops were designed to produce the standards; the first one for DECT and another one for GSM/ CDMA and NADC.

In synthesizers for stability of loop, Loop Band Width (LBW) should be less than $0.1\omega_{REF}$; with a big LBW phase noise of VCO can be eliminated in LOOP but with a small LBW phase noise of VCO can't be eliminated and appears at output. In integer-N synthesizers, ω_{REF} should be equal to ω_{CH}; therefore LBW is small and phase noise of VCO appears at output. But in fractional-N synthesizer ω_{REF} can be bigger than ω_{CH}, therefore ω_{REF} and LBW can be selected bigger, consequently phase noise of VCO can be eliminated. So in this paper fractional-N synthesizer with a big reference frequency was chosen in order to reduce the phase noise of output frequency. There are two main spur tones sources in PLL loops; the "reference spurs" and the "fractional spurs". The input reference frequency(ω_{REF}) modulates the VCO via clock feed trough of main switches of charge pump, generating sidebands around the center frequency, these sidebands are called " reference spurs" and repeats with ω_{REF} intervals [2-5].

$$v_{out} \approx V_m \cos\left[\omega_{FR} + K_{VCO}.\frac{\Delta V.\Delta t}{T_{REF}} + K_{VCO}V_1\right].t - K_{VCO}\left[V_m \sum_{n\neq 0} \frac{a_n}{n.\omega_{REF}}.\sin(n\omega_{REF}t + \theta_n)\right]. \sin\left[\omega_{FR} + K_{VCO}.\frac{\Delta V.\Delta t}{T_{REF}} + K_{VCO}V_1\right]t \quad (1)$$

Equation (1) shows these spur tones, where ω_{FR} is output frequency of VCO with $V_{cont}=0$, K_{VCO} is coefficient of VCO, T_{REF} is period of reference frequency, V_1 is DC level of V_{cont}, ΔV is amplitude of ripple of V_{cont}, Δt is period of ripple of V_{cont} and n is number\ of harmonics. The first sentence of equation (1) shows main carrier and second sentence shows the reference spur tones that repeats with ω_{REF} intervals and the magnitude of spur tones is proportional to $1/\omega_{REF}$; therefore using a big reference frequency (ω_{REF}) results reduction of reference spur tones magnitude [1-3].

In fractional synthesizer in addition to "reference spurs", N/N+1 divider modulates V_{cont} and then the VCO produces spur tones with $\alpha\omega_{REF}$ intervals called " fractional spurs". These spurs are more near the center frequency than reference spurs and more dangerous. These spur tones should be far from center frequency [2, 5]. In this paper a new "Channel Select circuit" was used instead of $\sum\Delta$ modulator to locate spur tones far from center frequency by means of two ways. In the first way output signal was used as clock. In the second way the time period that any division ratio is selected was reduced. A new T flip-flop was used in Channel Select circuit; this flip-flop uses a TSCP positive edge D flip-flop with a feedback circuit that has highspeed.

In section II, frequency plan for proposed standards and system architecture were introduced. Section III is about circuit design; in subsection "A"; LC-VCO along with phase noise improvement techniques were described; in subsection "B"; at first fundamental basis of channel select circuit was described then the designed circuit was introduced; in subsections of "C"; and "D" P.divider, 2-divider, multiplexer, phase frequency detector (PFD), charge pump (CP) and loop filter were introduced. Section IV contains simulation results and section V contains conclusions.

Frequency plan and system architecture

Table 1 shows frequency ranges and channel spaces of the DECT, GSM, CDMA and NADC standards. As you can see, the channel spaces are not an integer coefficient of each other (except in CDMA and NADC), so divider can't be used to obtain one standard from another; therefore we must design a frequency plan for each standard. When one reference frequency was used for each standard; in some standards (for example NADC) the number of clock pulse which is needed to perform a "phase comparison act" becomes very big, it leads to a big settling time. So in order to reduce the settling time, different reference frequencies were used; 86.4 MHz for DECT, 26 MHz for GSM900; 24.6 MHz for CDMA and NADC.

Table 1
Standards specifications.

Standard	Specifications		
	Uplink(MHz)	***Downlink(MHz)***	***Channel space***
DECT	1880-1900	1880-1900	1.728 MHz
GSM900	890-915	935-960	200 kHz
CDMA	824-849	869-894	1.23 MHz
NADC	824-849	869-894	30 kHz

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Fig. 1 shows architecture of proposed fractional-N synthesizer that consists of PFD, Charge Pump, VCO, 2divider, P.divider, Multiplexer and Channel Select blocks.

Feedback path consists of 2-divider and P.divider returns output signal to PFD block. Reference frequency (ω_{REF}) is compared with feedback of output signal (V_f) by PFD block. This block produces up and down signal proportional to phase and frequency difference between ω_{REF} and V_f. These up and down signals change control voltage (V_{cont}), consequently VCO output frequency is changed; so that the phase and frequency difference between ω_{REF} and V_f becomes less. This process repeats until the difference becomes zero, at this point PLL is locked.

The divider ratio of 10 and 11 for DECT, 17, 18 and 19 for GSM900; 16, 17 and 19 for CDMA (or NADC) are needed in programmable divider. Ratio of programmable divider is N or N+1 which is selected by means of MUX block; if sel="1" N goes to P.divider, if sel="0" N+1 goes to P.divider. Channel select circuit is used to produce "sel" from 2-dvider output. Sel is "1" for A pulse of 2-dvider output and "0" for B pulse of 2-dvider output.

Circuit designs

LC-VCO Circuit

VCO is the most important module in the frequency synthesizer system; because its performance directly determines system out of band phase noise. Two VCOs [2, 6] were designed as shown in Fig. 2; one of them oscillates form 1877 to 1902 MHz for DECT and another one with switched capacitor (C_u); when "select" is "0" oscillates from 899 to 1040 MHz for GSM900 and when select is "1" oscillates from 829 to 899 MHz for CDMA & NADC.

The switched capacitors [2] were used to reduce the VCO gain (K_{VCO}) because of declaration of VCO phase noise. Switches S_2 and S_3 inter the C_u to circuit and S_1 was used to reduce R_{on} resistance of S_2 and S_3, when C_u is in the circuit, it is used to prevent declaration of Q in tank circuit. Varactors was made by M_3 and M_4. A capacitor (C_1 or C_2) and a self-biased inverter (M_5, M_6 or M_7, M_8) were used at output to eliminate DC level of output signal. A tail current (I_{SS}) is used to enhance PSRR. Two ways were used for phase noise optimization [7, 8]; in the first way, phase noise was reduced by a low pass filter and a bypass capacitor (C_T) that eliminate thermal noise of tail current source.

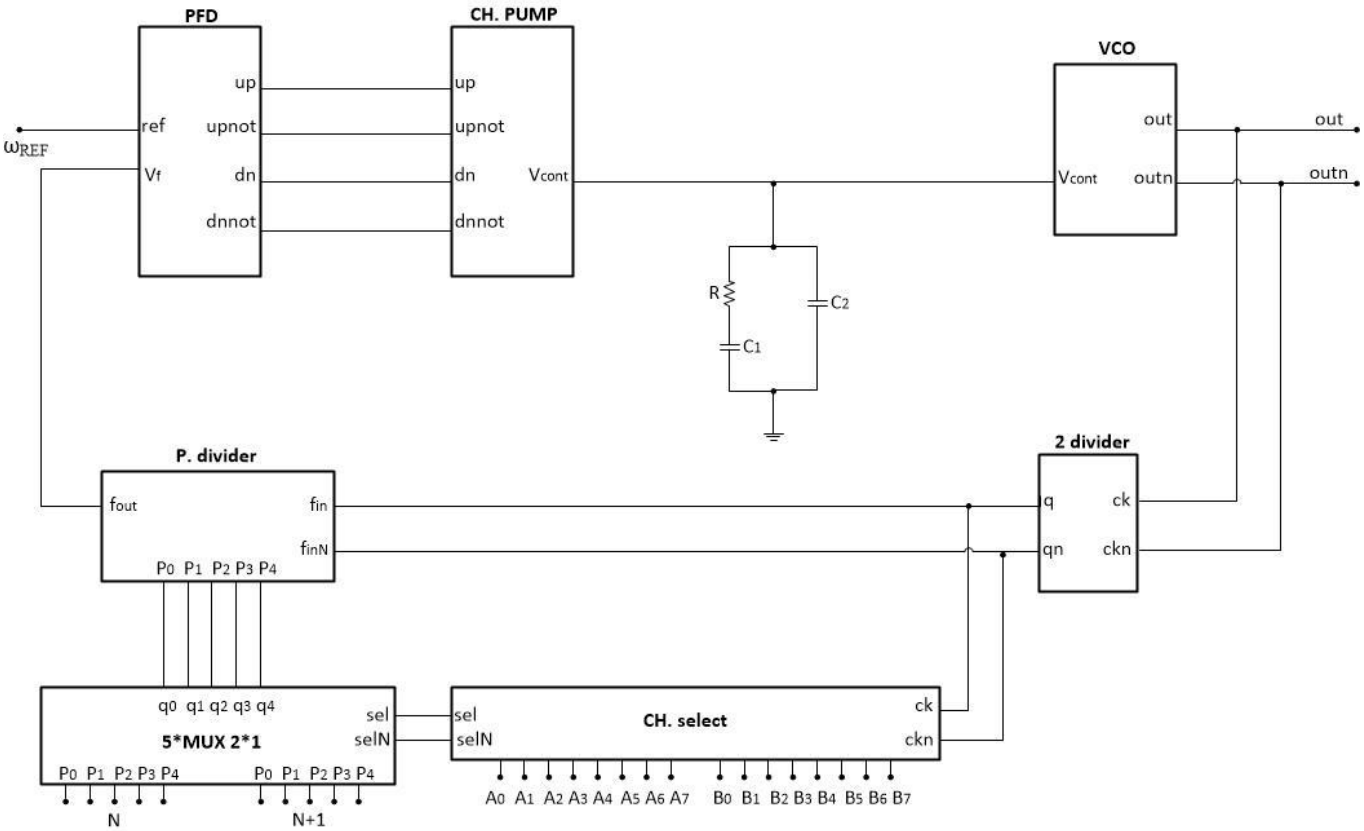

Figure 1. Architecture of proposed fractional-N synthesizer.

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In the second way, with biasing of VCO transistors only in saturation region preventing reduction of quality only in saturation region preventing reduction of quality factor(Q) in tank circuit. The C_T capacitor was used to eliminate $2\omega_0$ harmonics of I_{SS} and R_1, R_2, C_3, C_4 & V_b prevents M_1&M_2 from entrance to triode region (in order to prevent declaration of Q in tank circuit). These two ways in VCO of DECT were allpied, consequently the phase noise at 1875MHz center frequency was improved from -119.4 dBc/Hz at 3.4 MHz offset frequency to -144.3 dBc/Hz at 3.4 MHz offset frequency.

Channel select circuit

In fractional-N frequency synthesizer there are two division ratios, N and N+1. The N ratio is selected for "A" pulse and "B" ratio for N+1 pulse of reference frequency in order to produce α=B/(A+B) which is the fractional part of division ratio. The fractional spurs were produced because of this two division ratios. When division ratio is N, the period of reference and divider output are not equal so the V_{cont} starts to enhance; when division ratio is N+1, V_{cont} starts to reduce. So these variation in V_{cont} modulate (VCO) and produce fractional spur tones [2, 13].

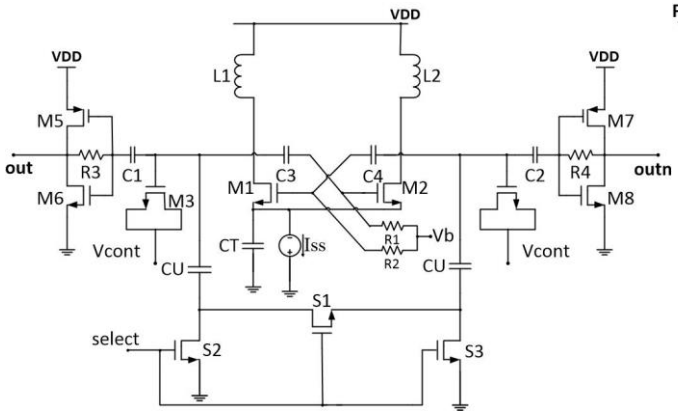

Figure 2. Schematic of the proposed VCO.

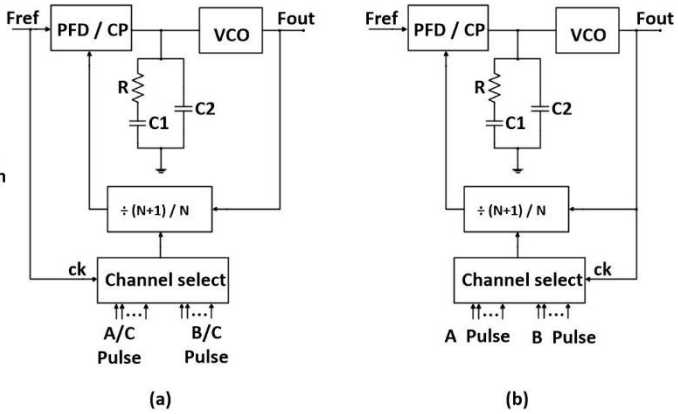

Figure 3. Channel select circuit fundamental basis.

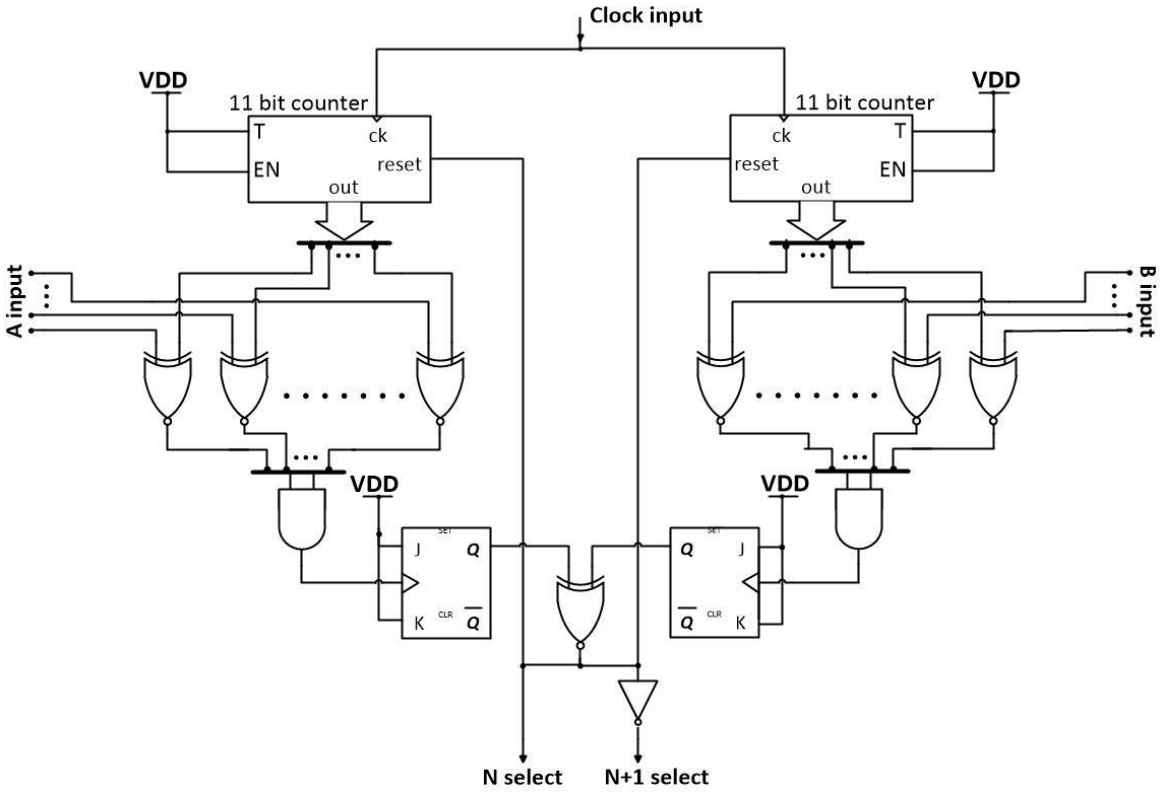

Figure 4. Channel select circuit fundamental basis.

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In order to locate spur tones far from center frequency; V_{cont} changes (ripple) should be reduced to prevent modulation of VCO. So each division ratio should be selected for a short time so the fractional part of division ratio(α) remains constant. In this paper, this act is done by means of "channel select circuit". By channel select circuit, two ways was used in order to reduce the time that each division ratio is selected. Fig. 3 shows these two ways. In the first way according to Fig. 3(a), A & B was divided by a constant digit(C), therefor N division ratio is selected for A/C pulse from reference, similarly N+1 is selected for B/C pulse from reference. So α remains constant and each division ratio is selected for a short time; consequently ripple of V_{cont} is reduced. In the second way according to Fig. 3(b), clock pulse for channel circuit was given from the output of synthesizer instead of reference frequency, so the period of each pulses and consequently the time that each division ratio is selected was shorten. By these two ways the ripple of V_{cont} can be reduced and fractional spur tones can be located far from center frequency.

A synchronous up counter was used as 11bit counter in channel select circuit. A new T flip-flop was used in this counter which is shown in Fig. 5. This flip-flop uses a TSCP positive edge D flip-flop [6, 9, 10] with a feedback circuit; when T="1" returns $\bar{Q}$ to D input and when T="0" returns Q to D input. The feedback circuit was made by M_{10}, M_{11}, M_{12}, M_{13} and two NOT gates in transmission gate logic. This T flip-flop has high speed.

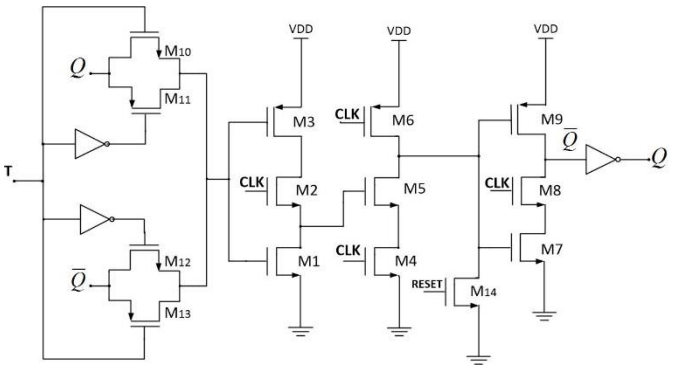

Figure 5. Schematic of new T flip-flop.

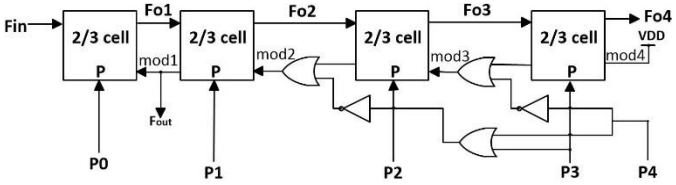

Figure 6. Programable divider

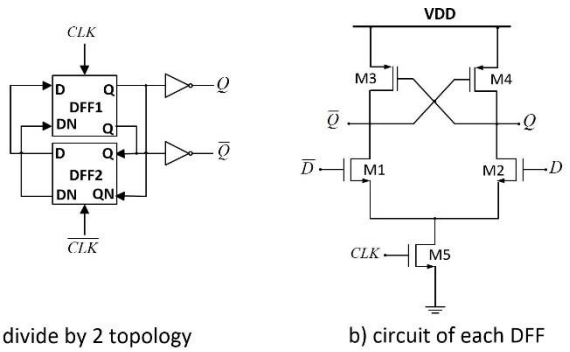

Figure 7. Proposed 2 divider.

Programmable and divide by 2 Dividers/multiplexer

Programmable divider [11] must have 10 and 11 ratio for DECT; 17, 18 and 19 for GSM900; 16, 17, 18 and 19 for CDMA(or NADC). Fig. 6 shows block diagram of a modular divider which is used in this paper. This divider has divide ratio of 4 to 31. Fig. 7 shows block and circuit diagram of 2divider [2, 6].

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PFD/CP/LPF

The characteristics of PFD and CP influence the PLL in-band noise dramatically. The reset pass delay of PFD should be short enough. In this work, a TSPC D flip-flop based PFD with a NOR gate in reset pass utilized in order to short reset time [12-14]. At charge pump, static and dynamic errors due to non-ideal effects of transistors were reduced using axillary switches in parallel with main switches. A cascade current source was used to set $I_{up} = I_{down}$ [1,3]. Also, a passive 2nd order loop filter was used [2, 4]. Equation (2) shows an approximate equation of settling time in PLL loops.

$$t_s \approx \frac{1}{\xi\omega_n}\ln\frac{k}{N_L|\lambda|\sqrt{1-\xi^2}} \qquad (2)$$

Where, N_L is the smallest divide ratio and k is difference between the smallest and the biggest divide ratio of divider in feedback path, λ is precision of output which is needed at output. In this paper, ξ was chosen "1" for loop filter design [2].

Simulation results

The proposed fast settling multi-standard fractional-N frequency synthesizer was simulated in 0.18µm CMOS technology. Two loops were simulated and favorite data was recorded. The whole frequency synthesizer in loop1 (for DECT) draws 13mA and in loop2 (for GSM900, CDMA & NADC) draws 13.67mA from a 1.8V power supply.
Fig. 8 shows the simulated phase noise of the DECT synthesizer in 1897 MHz center frequency. The phase noise is -116.37 dBc/Hz at 3 MHz offset frequency; settling time was measured 380 ns for DECT (Fig. 9).

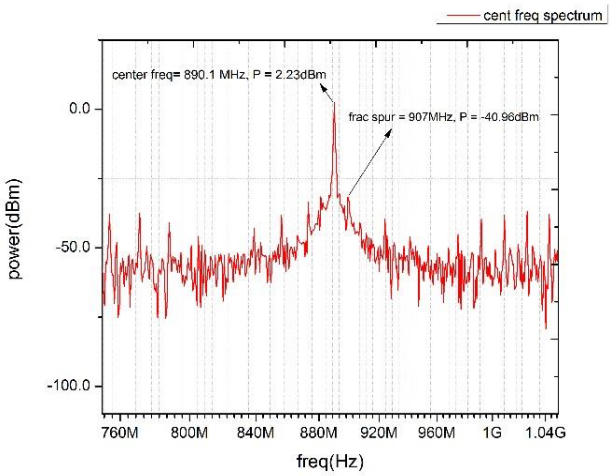

Figure 8. Simulated phase noise for DECT.

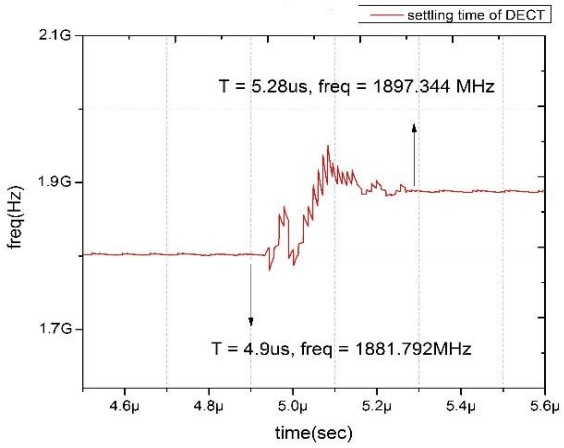

Figure 9. Simulated settling time in DECT.

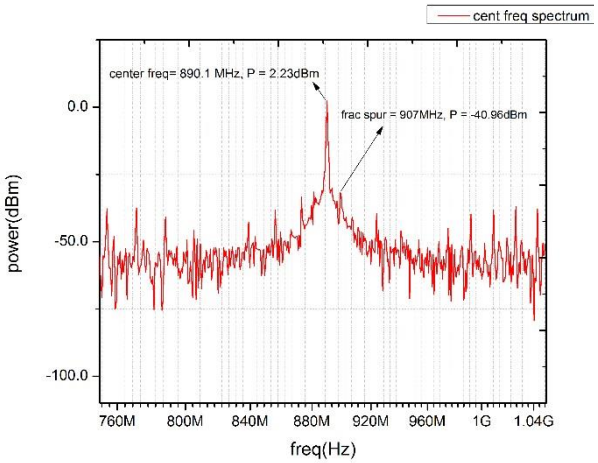

Figure 10. Simulated first spur tone for GSM900.

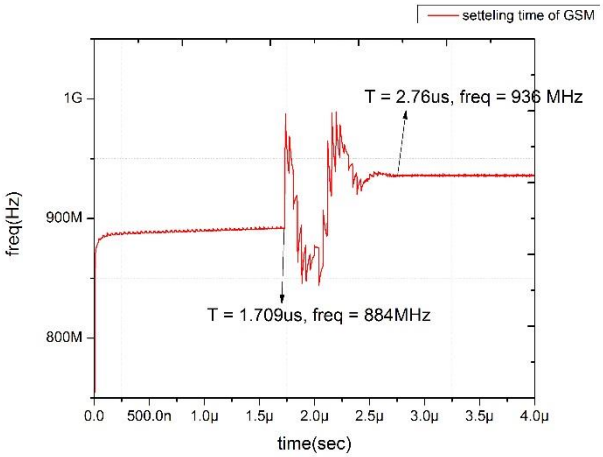

Figure 11. Simulated settling time in GSM900.

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In fractional-N synthesizers the first spur tone should be in frequency with $\alpha\omega_{ref}$ distance from center frequency; Fig. 10 shows the first channel of GSM transmitter (890.1 MHz); the first spur tone is located 16.9 MHz far from center frequency.

As mentioned, in the first channel of GSM transmitter with A=229 and B=31 and 890.1 MHz center frequency; the first spur without using the two ways (reducing the time that each division ratio is selected); should be in frequency with $\alpha\omega_{ref}$ =2.86 MHz distance from 890.1 MHz, but using these two ways, first spur was located farther. The phase noise is -111.57 dBc/Hz at 1.7 MHz offset frequency. According to Fig. 11, settling time was obtained 1051 ns for GSM900.

Fig. 12 demonstrates the simulated phase noise of CDMA synthesizer in 884.3 MHz center frequency.

The phase noise was obtained -116.3 dBc/Hz at 1.7 MHz offset frequency. According to Fig. 13, settling time was measured 700 ns for CDMA.

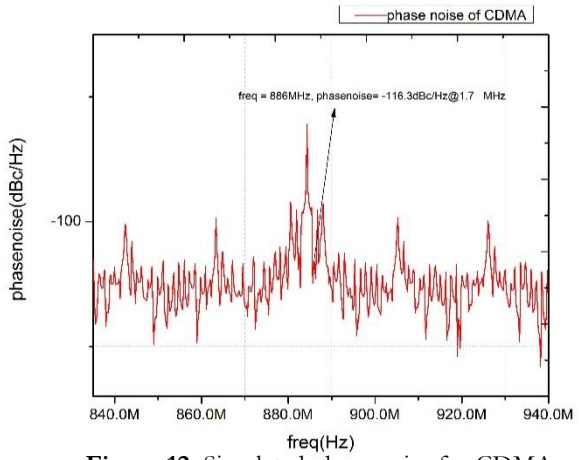

Figure 12. Simulated phase noise for CDMA.

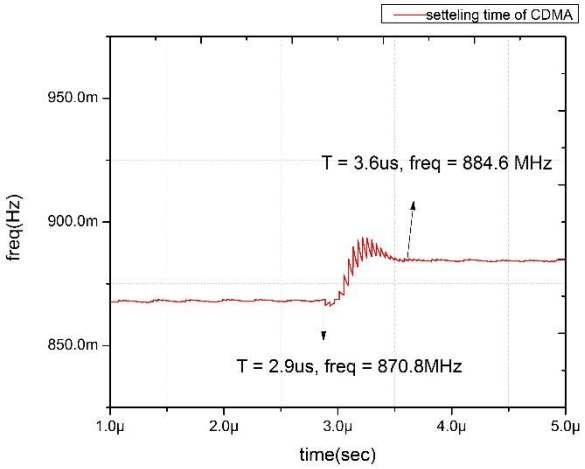

Figure 13. Simulated settling time in CDMA.

The simulated phase noise of the NADC synthesizer in 823.4 MHz center frequency is illustrated in Fig. 14. The phase noise was obtained -94 dBc/Hz at 1.4 MHz offset frequency. According to Fig. 15, the settling time was achieved 752 ns for NADC. Table II illustrates the result of proposed technique for DECT, GSM900, CDMA and NADC with comparison to other references.

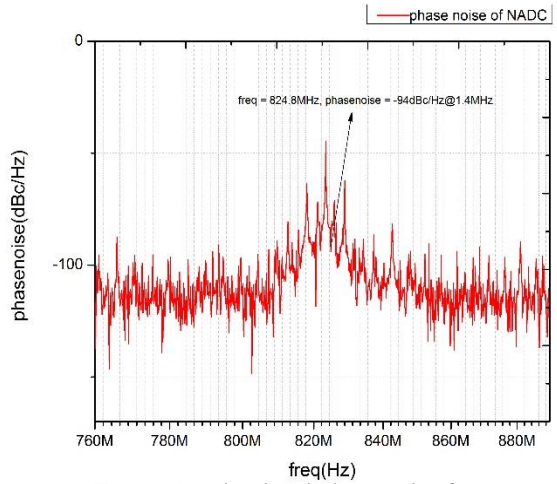

Figure 14. Simulated phase noise for NADC.

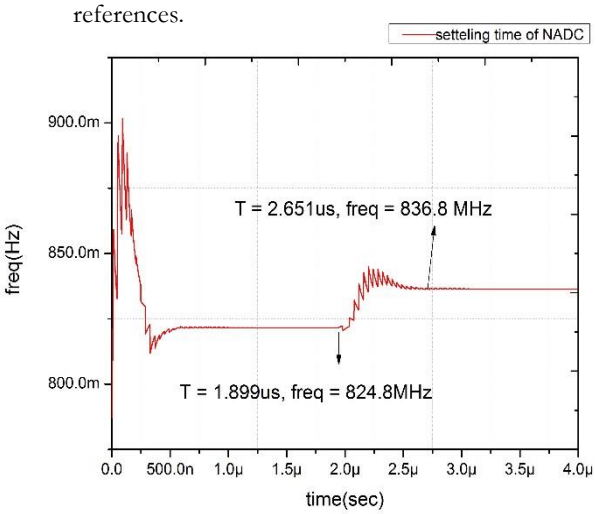

Figure 15. Simulated settling time in NADC.

Table 2
Simulation results and comparison.

*	DECT	GSM900	CDMA	NADC	[1]	[15]
V_{DD}	1.8 V	1.8 V	1.8 V	1.8 V	3.3 V	1.2 V
Technology	0.18 CMOS	0.18 CMOS	0.18 CMOS	0.18 CMOS	0.35 CMOS	0.13 CMOS
Phase noise dBc/Hz	−116.37 @3*MHz*	−111.57 @1.7*MHz*	−116.3 @1.7*MHz*	−94 @1.4*MHz*	−123 @3*MHz*	−132 @1*MHz*
Power	23.47 mW	24.6 mW	24.6 mW	24.6 mW	84.05 mW	-
$T_{settling}$	350 ns	1051 ns	700 ns	752 ns	-	22 µs

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Conclusion

A 1.8 V fast settling multi-standard CMOS fractional-N frequency synthesizer has been successfully simulated in a 0.18μm CMOS process. A novel "channel select circuit" employed instead of ∑Δ modulator to locate spurs tones far from center frequency. This circuit reduces the ripple of V_{cont} and consequently reduces modulation of VCO. A new T flip flop was employed in channel select circuit. The whole frequency synthesizer in loop1 (for DECT) draws 13 mA and in loop2 (for GSM900, CDMA & NADC) draws 13.67 mA from a 1.8 V power supply.

The proposed synthesizer for DECT achieved phase noise of -116.37 dBc/Hz at 3 MHz offset frequency and settling time was obtained 350 ns. The phase noise of reference frequency source of PLL, is about -155 dBc/Hz at 3.4 MHz offset frequency; the phase noise of VCO, is about -144.3 dBc/Hz at 3.4 MHz offset frequency and the phase noise of DECT was obtained -116.37 dBc/Hz at 3.4 MHz offset frequency which shows the VCO has added about -10.7 dBc/Hz phase noise at 3.4 MHz offset frequency to output signal which is a good performance for VCO and the rest of modules of PLL such as PFD, charge pump, loop filter and etc. have added about -27.33 dBc/Hz phase noise at 3.4 MHz offset frequency to output signal. Therefore these blocks should be optimized in order to add less noise.

The GSM900 proposed synthesizer achieved phase noise of -111.57 dBc/Hz at 1.7 MHz offset frequency, the first spur tone using channel select circuit was located in 16.9 MHz offset from center frequency instead of 2.86 MHz distance and settling time was obtained 1051 ns.

The proposed synthesizer for CDMA achieved phase noise of -116.3 dBc/Hz at 1.7 MHz offset frequency and settling time was obtained 700 ns. The proposed synthesizer for NADC achieved phase noise of -94 dBc/Hz at 1.4 MHz offset frequency and settling time was obtained 752 ns.

As mentioned two ways were used for phase noise optimization of VCO; low pass filter of I_{ss} and anti-triode circuit of main switch in charge pump. For example for VCO of DECT applying of these way improved VCO phase noise from -119.4 dBc/Hz at 3.4 MHz offset frequency to -144.3 dBc/Hz at 3.4 MHz offset frequency.

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