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Power Quality Improvement with T-Connected Transformer and Three-leg VSC Based DSTATCOM

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Abstract
Inthis paper, a new three-phase four-wire distribution static compensator (DSTATCOM) based on a T-connected transformer and a three-leg voltage source converter (VSC) is proposed for power quality improvement. The T-connected transformer connection mitigates the neutral current and the three-leg VSC compensates harmonic current, reactive power, and balances the load. Two single-phase transformers are connected in T-configuration for interfacing to a three-phase four-wire power distribution system and the required rating of the VSC is reduced. The insulated gate bipolar transistor (IGBT) based VSC is supported by a capacitor and is controlled for the required compensation of the load current. The dc bus voltage of the VSC is regulated during varying load conditions. The DSTATCOM is tested for power factor correction and voltage regulation along with neutral current compensation, harmonic elimination, and balancing of linear loads as well as nonlinear loads. The performance of the three-phase fourwire DSTATCOM is validated using MATLAB software with its Simulink and power system blockset toolboxes.

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Introduction:

Three-phase four-wire distribution grids are facing severe power quality problems such as poor voltage regulation, high reactive power and harmonics current burden, load unbalancing, excessive neutral current, etc. [1]–[5]. Three-phase four-wire distribution grids are used in commercial buildings, office buildings, hospitals, etc. Most of the loads in these locations are nonlinear loads and are mostly unbalanced loads in the distribution grid. This creates excessive neutral current both of fundamental and harmonic frequency, also the neutral conductor gets overloaded. The voltage regulation is also poor, due to the unplanned expansion and the installation of different types of loads in the existing distribution grid. In order to control the power quality problems, many standards are proposed, such as the IEEE-519 standard [6]. There are mitigation techniques for power quality problems in the distribution grid and the group of devices is known by the generic name of custom power devices (CPDs) [1]. The distribution static compensator (DSTATCOM) is a shunt-connected CPD capable of compensating power quality in the load current. Some of the topologies of DSTATCOM for three phase four-wire system for the mitigation of neutral current along with power quality compensation in the source current are four-leg voltage source converter (VSC), three single-phase VSCs, three-leg VSC with split capacitors [3], three-leg VSC with zig-zag transformer [7]–[9], and three-leg VSC with neutral terminal at the positive or negative of dc bus [10]. The voltage regulation in the distribution feeder is improved by installing a shunt compensator [11]. There are many control schemes reported in the literature for control of shunt active compensators such as instantaneous reactive power theory, power balance theory, synchronous reference frame theory, symmetrical components based, etc. [12], [13]. The synchronous reference frame theory [12] is used for the control of the proposed DSTATCOM.

In this paper, a new topology of DSTATCOM is proposed for a three-phase four-wire distribution system, which is based on three-leg VSC and a T-connected transformer. The T-connected transformer used in the three-phase distribution grid for different applications [14]–[16].But the application of T-connected

transformer for neutral current compensation is demonstrated for the first time. Moreover, the T-connected transformer is suitably
designed for magnetic motive force (mmf) balance. The T-connected transformer mitigates the neutral current and the three-leg VSC compensates the harmonic current and reactive power, and balances the load. The insulated gate bipolar transistor (IGBT) based VSC is self-supported with a dc bus capacitor and is controlled for the required compensation of the load current. The DSTATCOM is designed and simulated using MATLAB software with its Simulink and power system blockset (PSB) toolboxes for power factor correction and voltage regulation along with neutral current compensation, harmonic elimination, and load balancing with linear loads as well as nonlinear loads.

system configuration and design:

Fig. 1(a) shows the single-line diagram of the shunt-connected DSTATCOM-based distribution system. The dc capacitor connected at the dc bus of the converter acts as an energy buffer and establishes a dc voltage for the normal operation of the DSTATCOM system. The DSTATCOM can be operated for reactive power compensation for power factor correction or voltage regulation. Fig. 1(b) shows the phasor diagram for the unity power factor operation. The DSTATCOM injects a current *Ic* such that the source current is only *Is* , and this is in-phase with voltage. The voltage regulation operation of DSTATCOM is depicted in the phasor diagram of Fig. 1(b). The DSTATCOM injects a current *Ic* such that the voltage at the load (*VS*) is equal to the source voltage (*VM*).

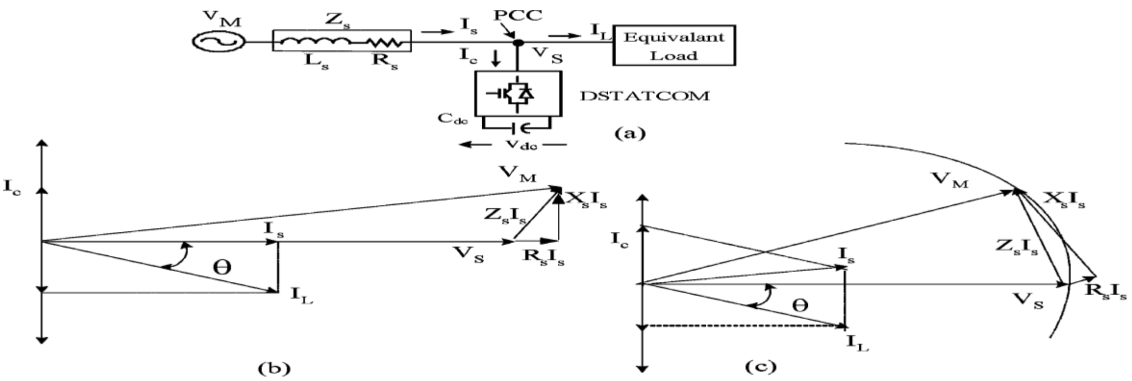

Fig. 1. (a) Single-line diagram of DSTATCOM system. (b) Phasor diagram for UPF operation. (c) ZVR operation.

The proposed DSTATCOM consisting of a three-leg VSC and a T-connected transformer is shown in Fig. 2, where the T-connected transformer is responsible for neutral current compensation. The windings of the T-connected transformer are designed such that the mmf is balanced properly in the transformer.
A three-leg VSC is used as an active shunt compensator along with a T-connected transformer, as shown in Fig. 2, and this topology has six IGBTs, three ac inductors, and one dc capacitor.
The required compensation to be provided by the DSTATCOM decides the rating of the VSC components. The data of DSTATCOM system considered for analysis is shown in the Appendix.
The VSC is designed for compensating a reactive power of 12 kvar, as decided from the load details. The selection of interfacing inductor, dc capacitor, and the ripple filter are given in the following sections.

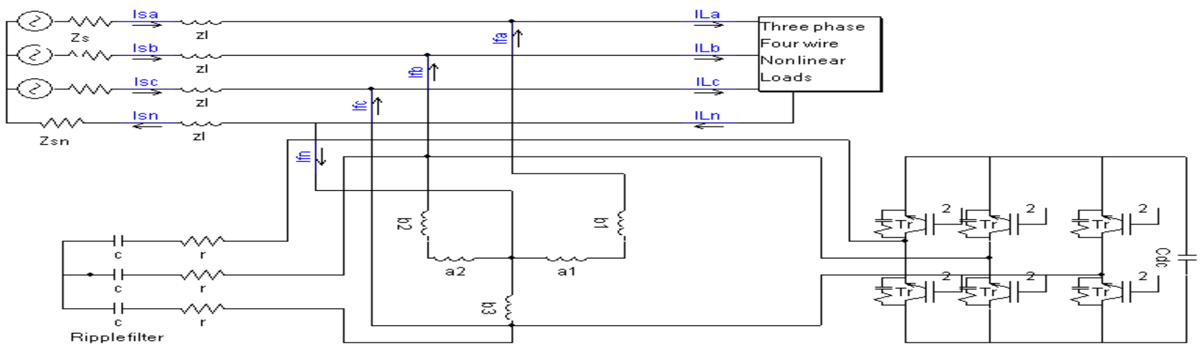

Fig. 2. Schematics of the proposed three-leg VSC with T-connected transformer- based DSTATCOM connected in distribution system.

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control of dstatcom:

The control approaches available for the generation of reference source currents for the control of VSC of DSTATCOM for three-phase four-wire system are instantaneous reactive power theory (IRPT), synchronous reference frame theory (SRFT), unity power factor (UPF) based, instantaneous symmetrical components based, etc. [12], [13]. The SRFT is used in this investigation for the control of the DSTATCOM. A block diagram of the control scheme is shown in Fig. 4. The load currents (*iLa, iLb, iLc*), the PCC voltages (*vSa, vSb, vSc*), and dc bus voltage (*v*dc) of DSTATCOM are sensed as feedback signals. The load currents from the *a–b–c* frame are first converted to the *α–β–o* frame and then to the *d–q–o* frame using

$$\begin{bmatrix} Id \\ Iq \\ Io \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos(\theta-120) & \cos(\theta+120) \\ \sin\theta & \sin(\theta-120) & \sin(\theta+120) \\ 0.5 & 0.5 & 0.5 \end{bmatrix}\begin{bmatrix} Ia \\ Ib \\ Ic \end{bmatrix} \quad (1)$$

where cos *θ* and sin *θ* are obtained using a three-phase phase locked loop (PLL). A PLL signal is obtained from terminal voltages for generation of fundamental unit vectors [18] for conversion of sensed currents to the *d–q–o* reference frame. The SRF controller extracts dc quantities by a low-pass filter, and hence, the non-dc quantities (harmonics) are separated from the reference signal. The *d*-axis and *q*-axis currents consist of fundamental and harmonic components as

$$I_{Ld} = I_{ddc} + I_{dac} \quad (2)$$
$$I_{Lq} = I_{qdc} + I_{qac} \quad (3)$$

The control strategy for reactive power compensation for UPF operation considers that the source must deliver the mean value of the direct-axis component of the load current along with the active power component current for maintaining the dc bus and meeting the losses (*i*loss) in DSTATCOM. The output of the proportional-integral (PI) controller at the dc bus voltage of DSTATCOM is considered as the current (*i*loss) for meeting its losses

*i*loss(*n*) = *i*loss(*n*−1) + *Kpd*(*vde*(*n*) −*vde*(*n*−1)) + *Kidvde*(*n*) (4)

where *vde*(*n*) = *v*∗dc −*v*dc(*n*) is the error between the reference (*v*∗ dc) and sensed (*v*dc) dc voltages at the *n*th sampling instant. *Kpd* and *Kid* are the proportional and integral gains of the dc bus voltage PI controller.

The reference source current is therefore

i∗*d* = *id* dc + *i*loss . (5)

The reference source current must be in phase with the voltage at the PCC but with no zero-sequence component. It is therefore obtained by the following reverse Park's transformation with *i*∗*d* as in (5) and *i*∗*q* and *i*∗0 as zero

$$\begin{bmatrix} Ia \\ Ib \\ Ic \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 1 \\ \cos(\theta-120) & \sin(\theta-120) & 1 \\ \cos(\theta+120) & \sin(\theta+120) & 1 \end{bmatrix}\begin{bmatrix} Id \\ Iq \\ Io \end{bmatrix} \quad (6)$$

The compensating strategy for ZVR operation considers that the source must deliver the same direct-axis component *i*∗*d*, as mentioned in (5) along with the sum of quadrature-axis current (*iq* dc) and the component obtained from the PI controller (*iqr*) used for regulating the voltage at PCC. The amplitude of ac terminal voltage (*VS*) at the PCC is controlled to its reference voltage (*V* ∗ *S*) using the PI controller. The output of PI controller is considered as the reactive component of current (*iqr*) for zero-voltage regulation of ac voltage at PCC. The amplitude of ac voltage (*VS*) at PCC is calculated from the ac voltages (*vsa*, *vsb*, *vsc*) as

$$V_S = \sqrt{\left(\left(\frac{2}{3}\right)(Va^2 + Vb^2 + Vc^2)\right)} \quad (7)$$

Then, a PI controller is used to regulate this voltage to a reference value as

iqr(*n*) = *iqr*(*n*−1) + *Kpq* (*vte*(*n*) −*vte*(*n*−1)) + *Kiq vte*(*n*) (8)

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where $vte(n) = V * S - VS(n)$ denotes the error between reference ($V * S$) and actual ($VS(n)$) terminal voltage amplitudes at the nth sampling instant. Kpq and Kiq are the proportional and integral gains of the dc bus voltage PI controller. The reference source quadrature-axis current is

$$i*q = iq\,\mathrm{dc} + iqr \quad (9)$$

The reference source current is obtained by reverse Park's transformation using (6) with $i*d$ as in (5) and $i*q$ as in (9) and $i*0$ as zero.
The gains of the controllers are obtained using the Ziegler–Nichols step response technique [19]. A step input of amplitude (U) is applied and the output response of the dc bus voltage is obtained for the open-loop system. The maximum gradient (G) and the point at which the line of maximum gradient crosses the time axis (T) are computed. The gains of the controller are computed using the following equations:

$$Kp = 1.2U/GT \quad (10)$$

$$Ki = 0.6U/GT2. \quad (11)$$

The gain values for both the PI controllers are computed and are given in the Appendix.
In a current controller, the sensed and reference source currents are compared and a proportional controller is used for amplifying current error in each phase before comparing with a triangular carrier signal to generate the gating signals for six IGBT switches of VSC of DSTATCOM.

Simulation:
The three-leg VSC and the T-connected-transformer-based DSTATCOM connected to a three-phase four-wire system is modeled and simulated using the MATLAB with its Simulink and PSBs. The ripple filter is connected to the DSTATCOM for filtering the ripple in the PCC voltage. The system data are given in the Appendix. The MATLAB-based model of the three-phase four-wire DSTATCOM is shown in Fig. 5. The T-connected transformer in parallel to the load, the three-phase source, and the shunt-connected three-leg VSC are connected as shown in Fig. 5. The available model of linear transformers, which includes losses, is used for modeling the T-connected transformer.
The control algorithm for the DSTATCOM is also modeled in MATLAB. The reference source currents are derived from the sensed PCC voltages (vsa, vsb, vsc), load currents (iLa, iLb, iLc), and the dc bus voltage of DSTATCOM ($v$dc). A PWM current controller is used over the reference and sensed source currents to generate the gating signals for the IGBTs of the VSC of the DSTATCOM.
In the first control block, the reference currents are obtained, that it should be compared with the original currents, then using the difference between this two, be sent pulses required for gate of the thyristor in DSTATCOM. In Figure shown the control block of phase a, also the required pulse for g1. That this pulse such be sent, until with in spite of non-linear and unbalanced load at the end of the line,are sinusoidal voltages and currents of each phase at the beginning of the line. Also should be fixed the DC capacitor voltage at 300 volts. In figure 5 is shown circuit system.

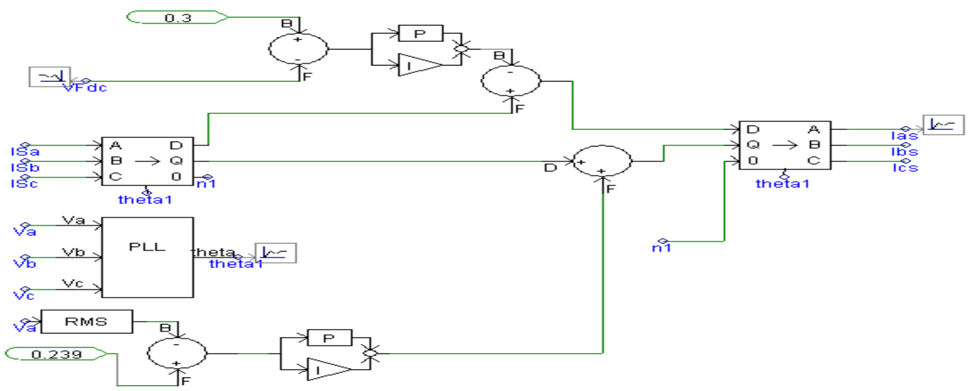

Figure 3. Block diagram of the control circuit

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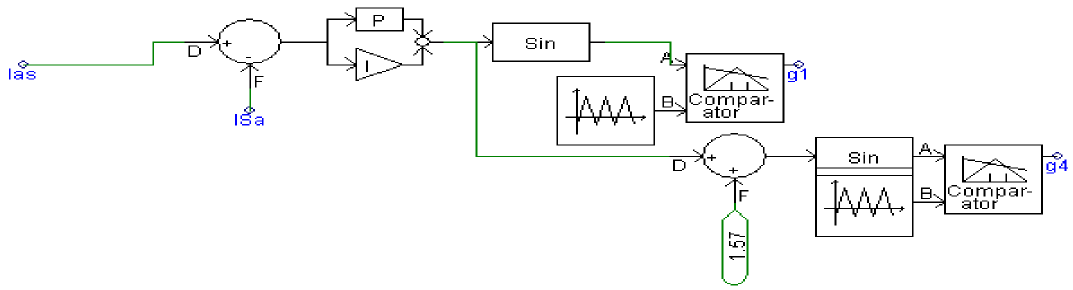

Figure 4: The control block, generating a reference current, pulse production

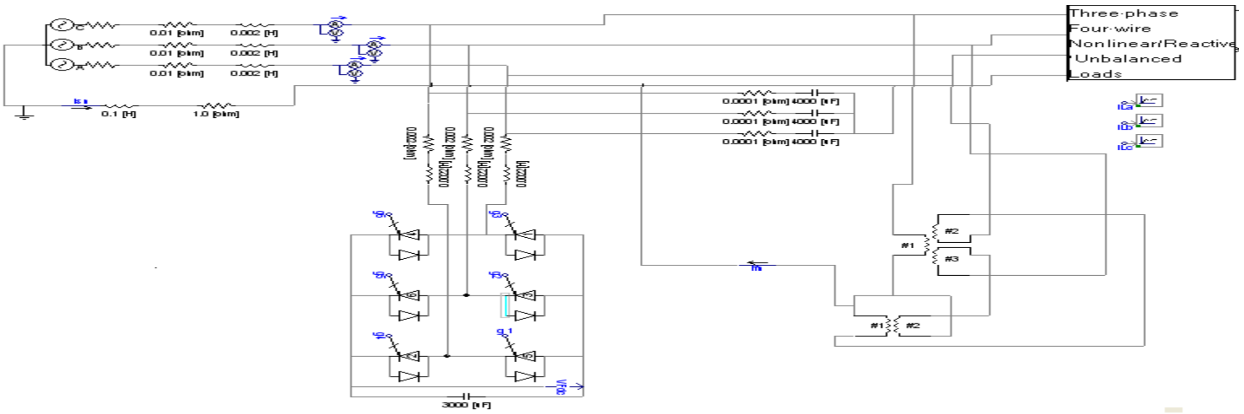

Figure 5: Three-phase four-wire system with DSTATCOM and VSC tripod and Transformer T-shaped simulated in PSCAD / EMTDC

Considering that our load is a non-linear load and load current is non-sinusoidal, thus current source and voltage source are non-sinusoidal and have the many harmonics. The performance of the T-connected transformer and threeleg- VSC-based three-phase four-wire DSTATCOM is demonstrated for power factor correction and voltage regulation along with harmonic reduction, load balancing, and neutral current compensation. The developed model is analyzed under varying loads and the results are discussed shortly. For this purpose to remove the harmonics are used the above circuits. In this circuit, of the fourth second the DSTATCOM is removed the circuit, that the following figures are the impact shown effect of DSTATCOM. In figure 6 is shown voltage source waveform, that from the fourth second was removed from circuit.

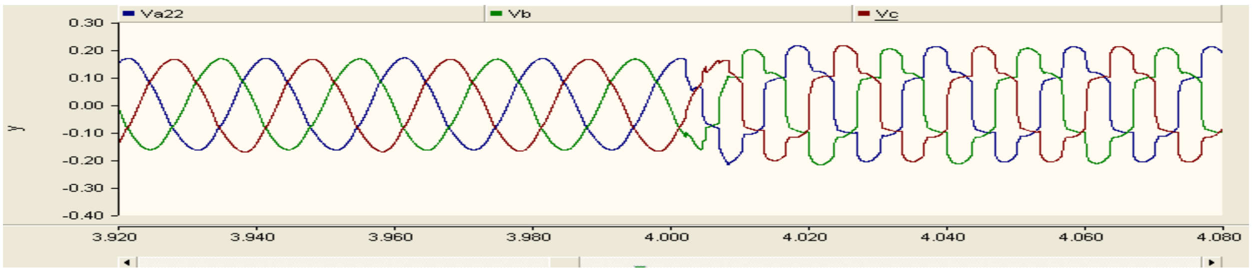

Figure 6: A part of the supply voltage waveform

In figure 7 shows the current source waveform with using of DSTATCOM will be fully sinusoidal, and in fourth second DSTATCOM is remove from circuit.

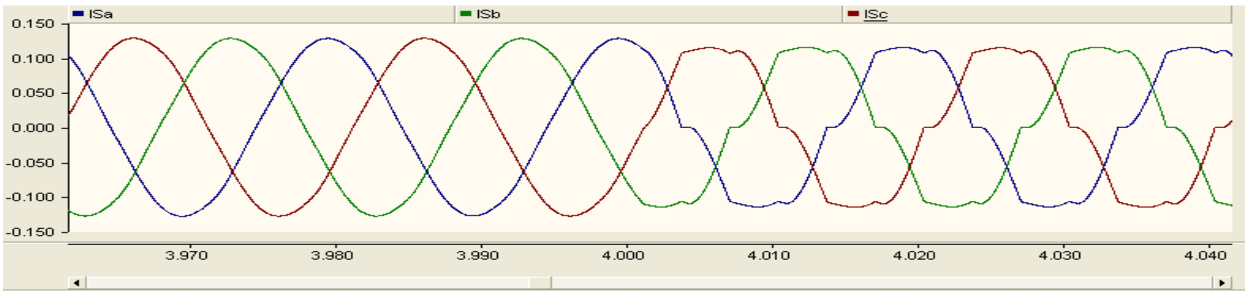

Figure 7: A part of the supply current waveform

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Figure 8 shows the waveform of the load current, that feeds the non-linear load.

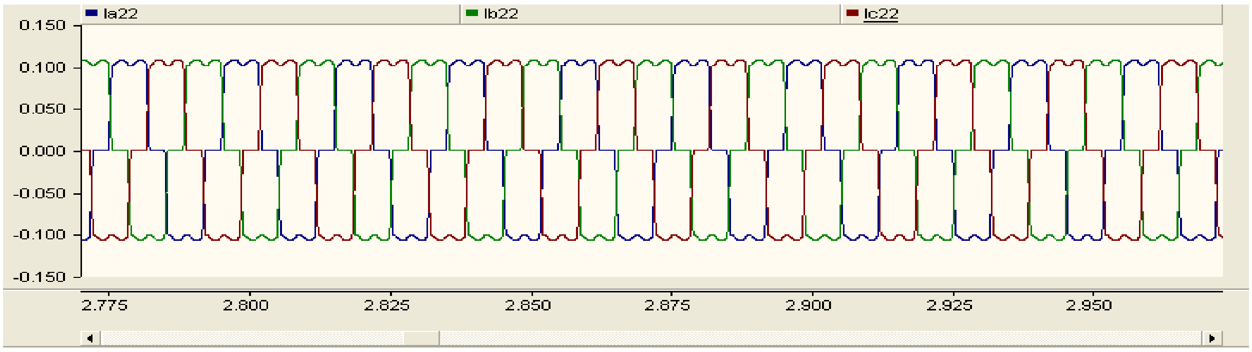

Figure 8: Part of the load current waveform

Dc capacitor voltage waveform which should be established on 300 volts shown in figure 9.

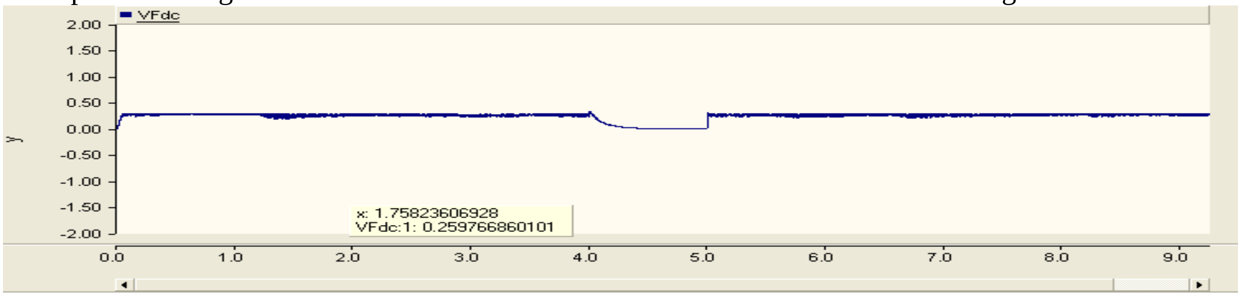

Figure 9: dc capacitor voltage

As mentioned is used T-form transformotor for eliminate the current of neutral line. In the diagram of figure 10 are shown the current of neutral wire in source side and load side. As expected, both sides of the neutral current is zero.

Figure 10: Waveform of the neutral wire in load And source side

In figure 11, is shown the current reference waveform which is generated by the control bloch. Also in figure 12 is shown the currents is given to the circuit with DSTATCOM.

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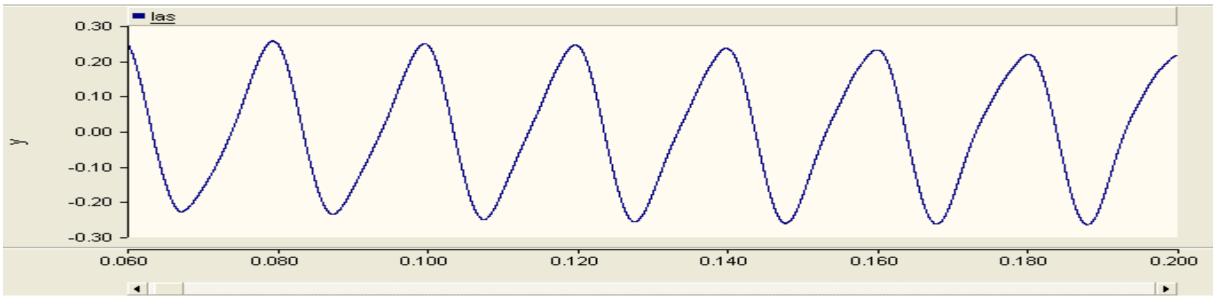

Figure 11. Waveform current reference

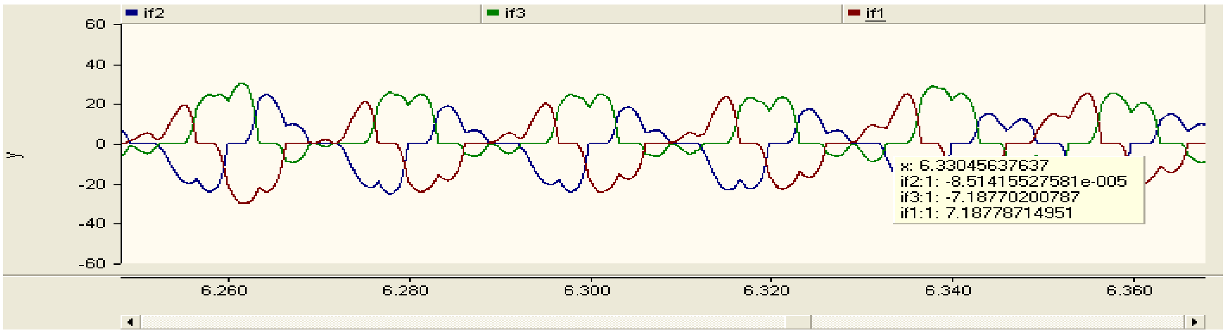

Figure 12 waveform currents D-STATCOM

And the simulation results are as follows:

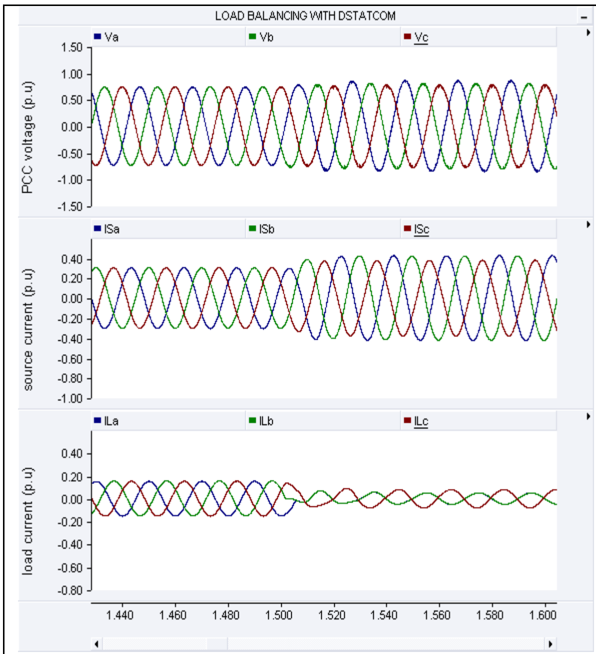	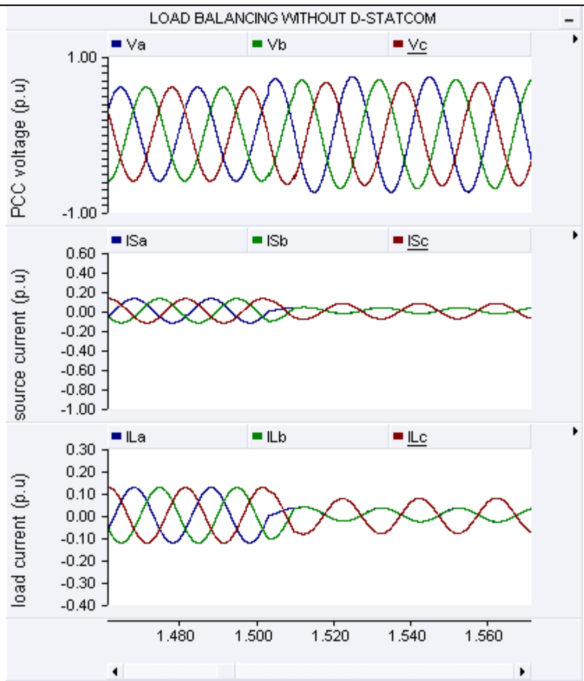
Figure 14.Voltage PCC, current source and the current load when the load will become from the three-phase mode to the one phases mode, in the three-phase four-wire system with D-STATCOM	Figure 13.Voltage PCC, current source and the current load when the load will become from the three-phase mode to the two phases mode, in the three-phase four-wire system no D-STATCOM

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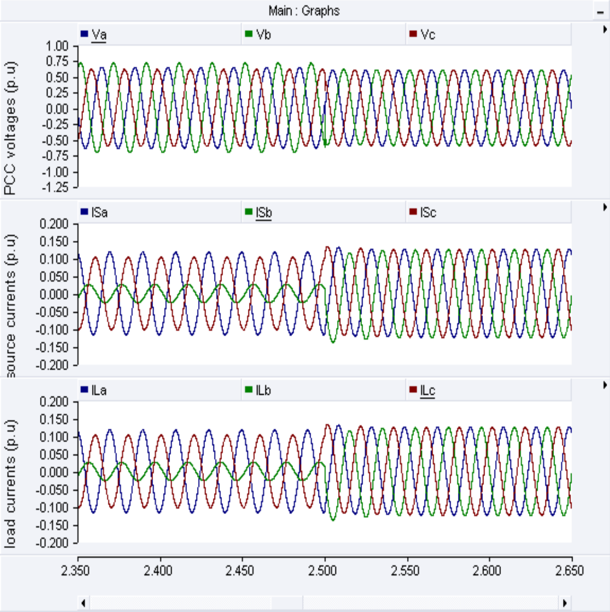

Figure 16.Voltage PCC, current source and the current load when the load will become from the two-phase mode to the three phases mode, in the three-phase four-wire system no D-STATCOM

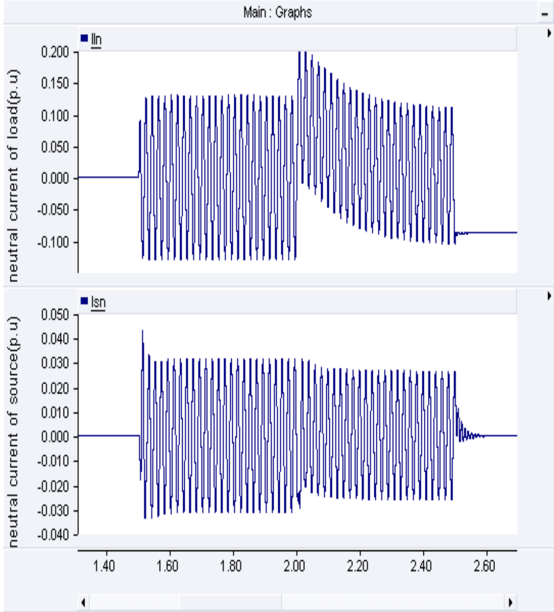

Figure 15. current of neutral load point and load source when the load will become from the three-phase mode to the one phases mode, in the three-phase four-wire system with D-STATCOM

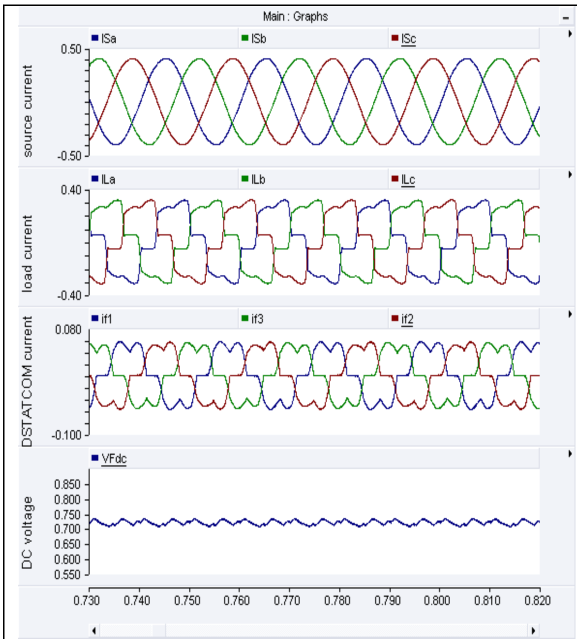

Figure 18. current of the source, load and D-STATCOM, and DC bus voltage in the presence of D-STATCOM in the three-phase four-wire system

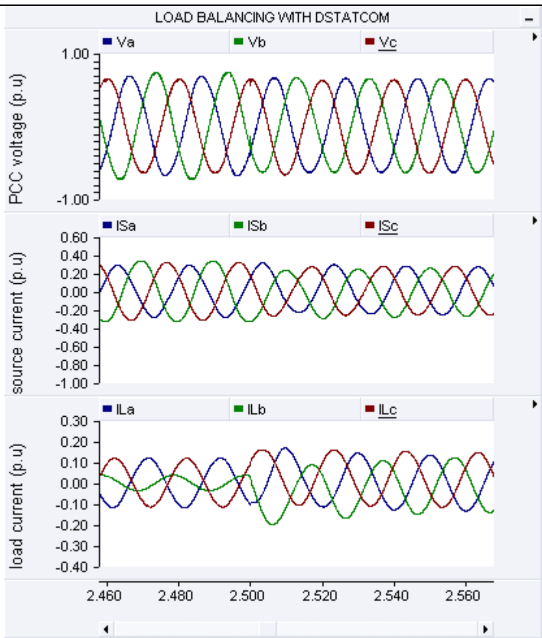

Figure 17.Voltage PCC, current source and the current load when the load will become from the two-phase mode to the three phases mode, in the three-phase four-wire system with D-STATCOM

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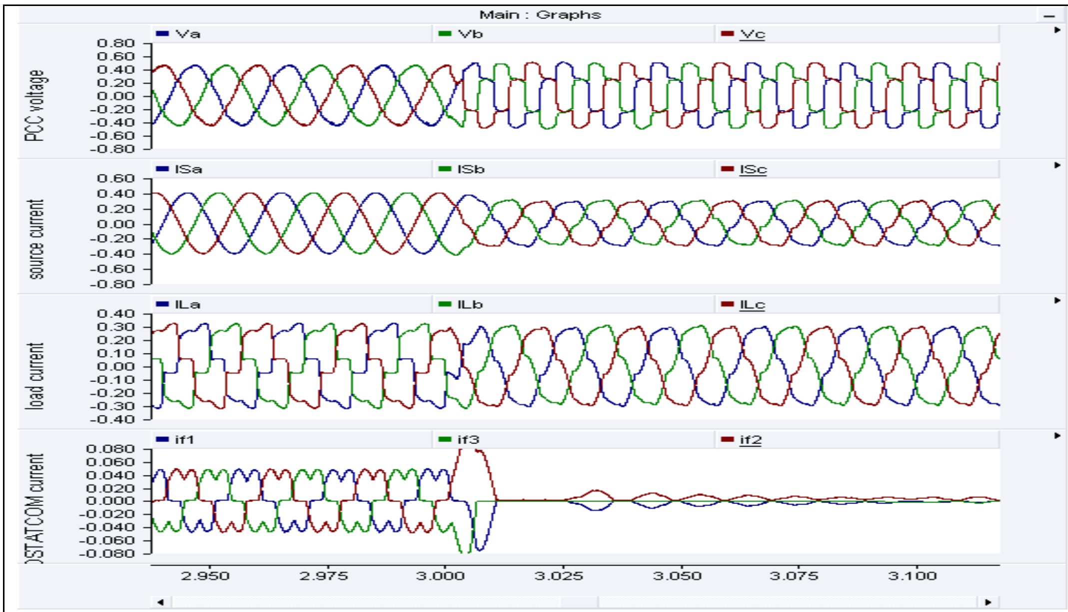

Figure 19. Voltage PCC, current source and the current load when D-STATCOM the circuit is removed At the time of 3 seconds in the three-phase four-wire system

Conclusion:

The performance of a new topology of three-phase four-wire DSTATCOM consisting of three-leg VSC with a T-connected transformer has been demonstrated for neutral current compensation along with reactive power compensation, harmonic elimination, and load balancing. The T-connected transformer has mitigated the source-neutral current. The voltage regulation and power factor correction modes of operation of the DSTATCOM have been observed and are as expected. The dc bus voltage of the DSTATCOM has been regulated to the reference dc bus voltage under all varying loads. Two single phase transformers are used for the T-configuration of the transformer to interface with a three-phase four-wire system. The total kilovolt· amperes rating of the T-connected transformer is lower than a star/delta transformer for a given neutral current compensation. The experimental results on a prototype have verified that the T-connected transformer has been effective in compensating the zero sequence fundamental and harmonics currents.

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